

Application Note

Methodology for Controlling Multi-Level Converter Topologies with SCALE™-2 IGBT Drivers

Introduction

This Application Note describes the methodology for controlling multi-level converter topologies with SCALE™-2 IGBT drivers in case of a fault. Multi-level converters use series-connected IGBTs to increase the amplitude and reduce the total harmonic distortion of the voltage and current output of the converter.

The basic topology of a multi-level converter requires dedicated turn-on and turn-off sequences to ensure that the collector-emitter voltage of the IGBTs does not exceed a predefined level. As a general rule, the outer IGBTs of a half-bridge should always be turned-off first (IGBTs S1 and S4 in Fig. 1). In case of a fault turn-off, it is essential either to implement the regular sequence or to apply an alternative sequence combined with additional ways of limiting the collector-emitter voltage and turn-off energy of the IGBTs.

Proposed Methodology with SCALE-2 Drivers

A dedicated turn-off sequence is not required in the event of a reported fault condition (e.g. short-circuit) using SCALE-2 drivers with Advanced Active Clamping (AAC). As soon as an IGBT driver detects a fault condition, it turns off the corresponding IGBT switch immediately (or with a corresponding delay /1/) regardless of its position in the converter topology, and a fault signal is transmitted to the user interface within a short time /1/. If an incorrect turn-off sequence is then applied, the AAC safely limits the maximum V_{ce} voltage of the corresponding IGBT. The host controller only needs to apply a common turn-off pulse to all IGBTs to avoid thermal overload of the IGBTs and IGBT drivers as soon as the driver fault is reported.

Several measurements shown below have been performed to highlight this fact.

Performed Investigations

Several investigations were performed using an Infineon F3L200R07PE4 650V/200A 3-level NPC1 IGBT module with a 2SC0108T2D0-07 SCALE-2 driver in a 3-Level NPC Topology according to Fig. 1. Refer to /2/ for more details. The typical TVS breakdown voltage is set to 479V at 1mA/25°C to allow a maximum DC-link voltage V_{dc} of 870V (both half DC-link voltages are set to the same value for all measurements). Two different short-circuit scenarios are considered.

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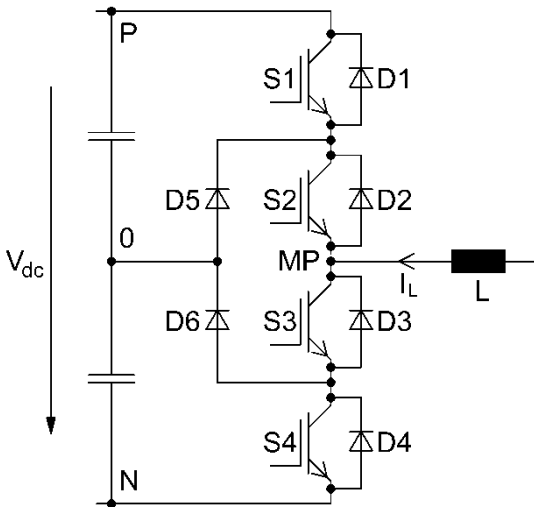


Fig. 1 3-level NPC topology

Short Circuit between Middle Point (MP) and Neutral Point (0)

A short-circuit path is introduced between the middle point MP and the neutral point 0 in the topology of Fig. 1. The measurement shown in Fig. 2 is performed with the maximum DC-link voltage V_{dc} of 870V.

Initially, all switches are in the off-state (a). IGBT S3 is then turned on (b). The half DC-link voltage of 435V is applied to IGBT S4 (V_{ce4}), and no short-circuit current flows. When S4 is turned on (c), the short-circuit current I_{c4} increases through S3 and S4 until IGBT S3 desaturates, followed a little later by S4. A dedicated turn-off sequence would require turning off IGBT S4 prior to S3. But S3 is turned off first (d). Without protective measures, the short-circuit current would commute to the diodes D1 and D2 in Fig. 1, leading to the full DC-link voltage of about 870V being applied to S3 (V_{ce3}), thus considerably exceeding the maximum IGBT voltage capability. Fig. 2 clearly shows the voltage limitation of V_{ce3} to a maximum value of 500V during the full turn-off phase (d). When the short-circuit current is completely turned off, the half DC-link voltage of 435V is applied to IGBT S3 (e).

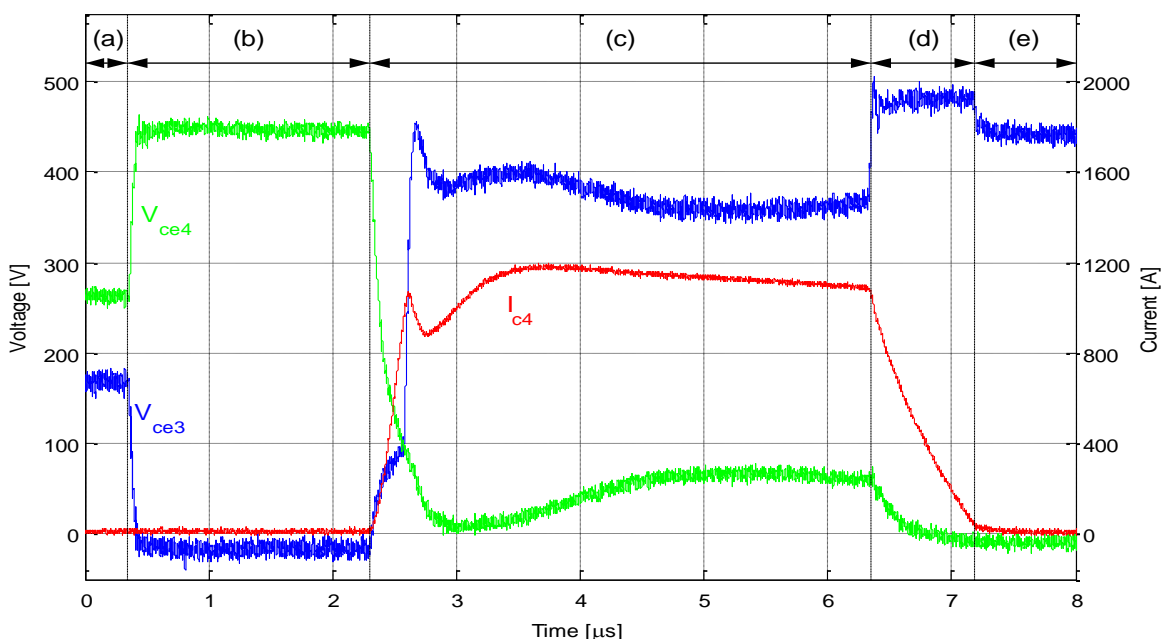


Fig. 2 "Incorrect" turn-off sequence during short circuit between MP and 0

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Short Circuit between Middle Point (MP) and DC-link Plus (P)

A short-circuit path is now introduced between the middle point MP and the DC-link plus (P) in the topology of Fig. 1. The measurement shown in Fig. 3 is performed with a DC-link voltage V_{dc} of 550V.

Initially, all switches are in the off-state (a). IGBT S3 is then turned on (b). A short-circuit current I_L begins to flow from P to MP, flowing further through S3 and D6. Half of the DC-link voltage V_{dc} is applied to IGBT S4 (V_{ce4}). About $1\mu s$ later, S4 is turned on (c). The short-circuit current commutates quickly from D6 to S4 (increase of I_{c4}). When IGBT S3 desaturates, its current is strongly reduced due to the short-term V_{ce3} over-voltage (not shown in Fig. 3). As the short-circuit current I_L remains relatively stable due to its inductive behavior (the short-circuit path possesses a minimum inductance), a current flow effectively equal to $I_L - I_{c4}$ is produced through diodes D1 and D2 during the entire phases (d), (e) and (f), i.e. the current $I_L - I_{c4}$ is freewheeling through D1 and D2. The full DC-link voltage V_{dc} is consequently applied between MP and N. AAC safely limits the voltage V_{ce3} to about 500V during this time (V_{ce3} is higher shortly after the desaturation of S3, but does not exceed IGBT RBSOA). The difference between the DC-link voltage V_{dc} and V_{ce3} , approximately equal to $550V - 500V = 50V$, is applied over the stray inductances available between MP, S3, S4 and N, as S4 is still saturated, which leads to a further increase of I_{c4} , although at a reduced rate (d).

When S4 desaturates (e), the current I_{c4} stops increasing. A dedicated turn-off sequence would require S4 to be turned off first. In fact, however, S3 is turned off first (f). The effect is almost imperceptible, as shown in Fig. 3. The reason is simple: AAC already limits the V_{ce3} voltage, which cannot therefore increase any further. The driver tries to reduce the gate-emitter voltage of S3, but the AAC function prevents this action. The IGBT S4 is then turned off (g) and I_{c4} ramps quickly down to zero. The corresponding V_{ce4} voltage is safely limited by the AAC of S4. The initial short-circuit current I_L then decreases over time by freewheeling through D1 and D2, as partly shown in Fig. 3 (g).

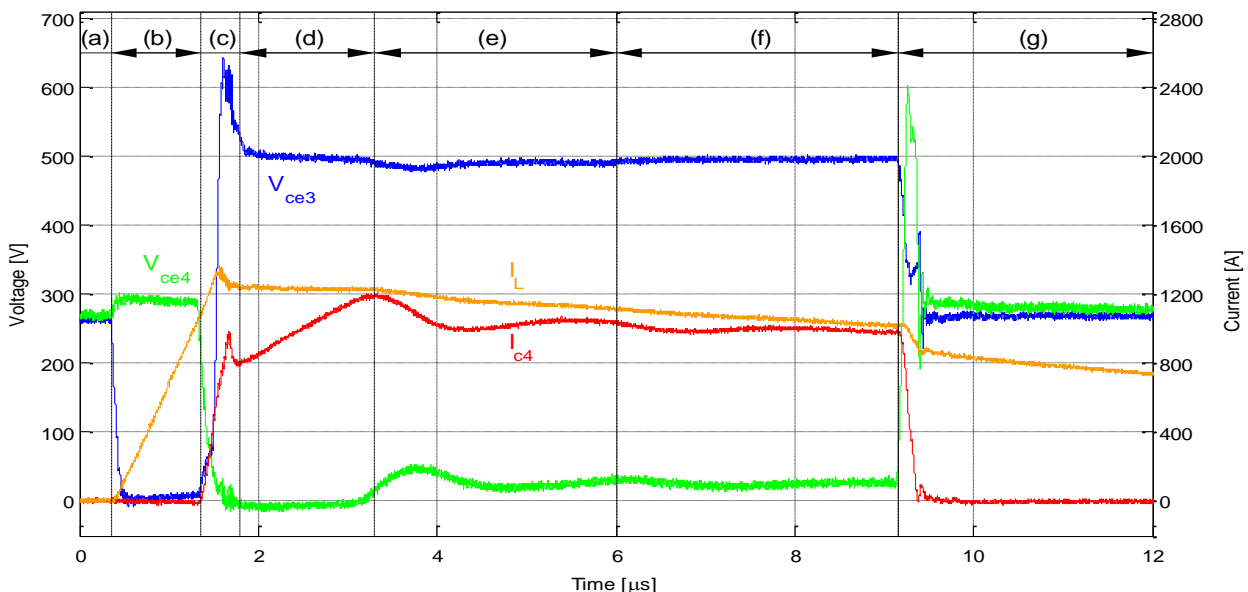


Fig. 3 "Incorrect" turn-off sequence during short-circuit between MP and P

Bibliography

- /1/ Data sheets of SCALE™-2 drivers, CONCEPT
- /2/ Paper: Safe Driving of Multi-Level Converters Using Sophisticated Gate Driver Technology, PCIM Asia, June 2013

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Legal Disclaimer

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Manufacturer

CT-Concept Technologie GmbH
A Power Integrations Company
Johann-Renfer-Strasse 15
2504 Biel-Bienne
Switzerland

Phone +41 - 32 - 344 47 47
Fax +41 - 32 - 344 47 40

E-mail Info@IGBT-Driver.com
Internet www.IGBT-Driver.com

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